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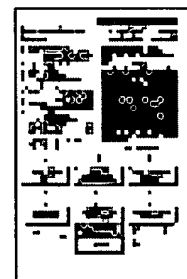
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 Inventor: **MAEDA AKIRA;
FUNABASHI SEIJU;
YAMAOKA HIROMASA;
FUJIKURA NOBUYUKI;
YODA MIKIO;
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ICHIMORI TOSHIHIDE;**

 Assignee: **HITACHI LTD**
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Published / Filed: **1994-05-20 / 1993-08-20**Application Number: **JP1993000206143**
 IPC Code: Advanced: **G06F 9/44; G06F 15/18; G06G 7/60; G05B 13/02;**
 Core: **G06G 7/00;** more...
 IPC-7: **G05B 13/02; G06F 9/44; G06F 15/18; G06G 7/60;**
Priority Number: **1992-09-08 JP1992000239258**
 Abstract: **PURPOSE:** To facilitate the designing and to provide high-level functions for high-speed processing, learning, etc., by storing plural pairs of values of input data and values of corresponding output data and determining an output on the basis of the pairs.

CONSTITUTION: Respective memory cells 103 are stored with the pairs of the input data (response pattern data) and output data. The respective memory cells 103 receive the input data distributed from a main CPU 102 and distance calculation parts 105 calculate distances to the response pattern data stored in the cells. The memory cells 103 outputs the output data to a data bus 101 through interface parts 104 according to the calculated distances. The main CPU 102 gathers the outputs from the respective memory cells 103 and puts the respective output data together by a weighted mean value method based upon the calculated distances to generate the final output.

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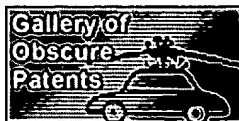
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